High-Speed CAN Transceiver

Features

- Very Low Standby Current (5 μA，typical)
- Suitable for 12 V and 24 V systems
- VIO Supply Pin to interface Directly to CAN Controllers and MCU with 1.8V to 5.5V I/O
- SPLIT Output Pin to Stabilize Common Mode in Biased Split Termination Schemes
- CAN Bus Pins are Disconnected when Device is Unpowered
- Bus Glitch-Free Power-Up and Power-Down
- Over Temperature Protection
- Allow Up to 128 Transceivers on the bus
- Data Rate Up to 5Mbps
- Half-duplex Transceiver
- Available Packaging: SOP8/DFN8/DIP8

Applications

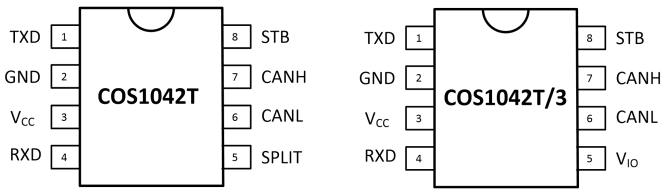
- Industrial Automation, Control
- CAN Networks

General Description

The COS1042 is a high-speed CAN, fault tolerant transceiver. It serves the interface between a Controller Area Network (CAN) protocol controller and the physical two-wire CAN bus. The COS1042 provides differential transmit and receive capability for the CAN protocol controller, and is fully compatible with the ISO-11898-2 and ISO-11898-5 standards.

The COS1042 can be interfaced directly to micro-controllers with supply voltages from 1.8V to 5.5V. It has a passive behavior to the CAN bus when the supply voltage is off.

The COS1042 has a very low-current standby mode with bus wake-up capability. It enables reliable communication in the CAN FD fast phase at data rates up to 5 Mbit/s.



Pin Diagram

Rev1.0

1. Pin Configuration and Block Diagram

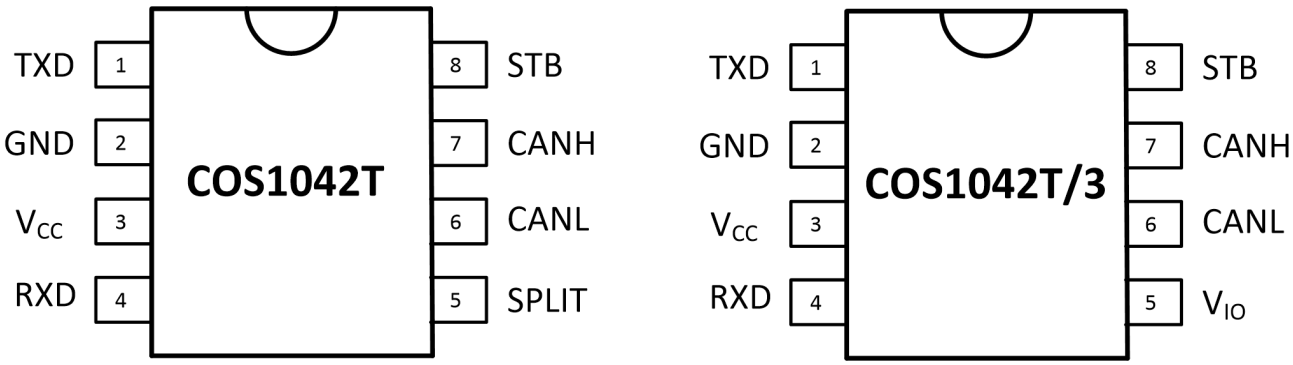


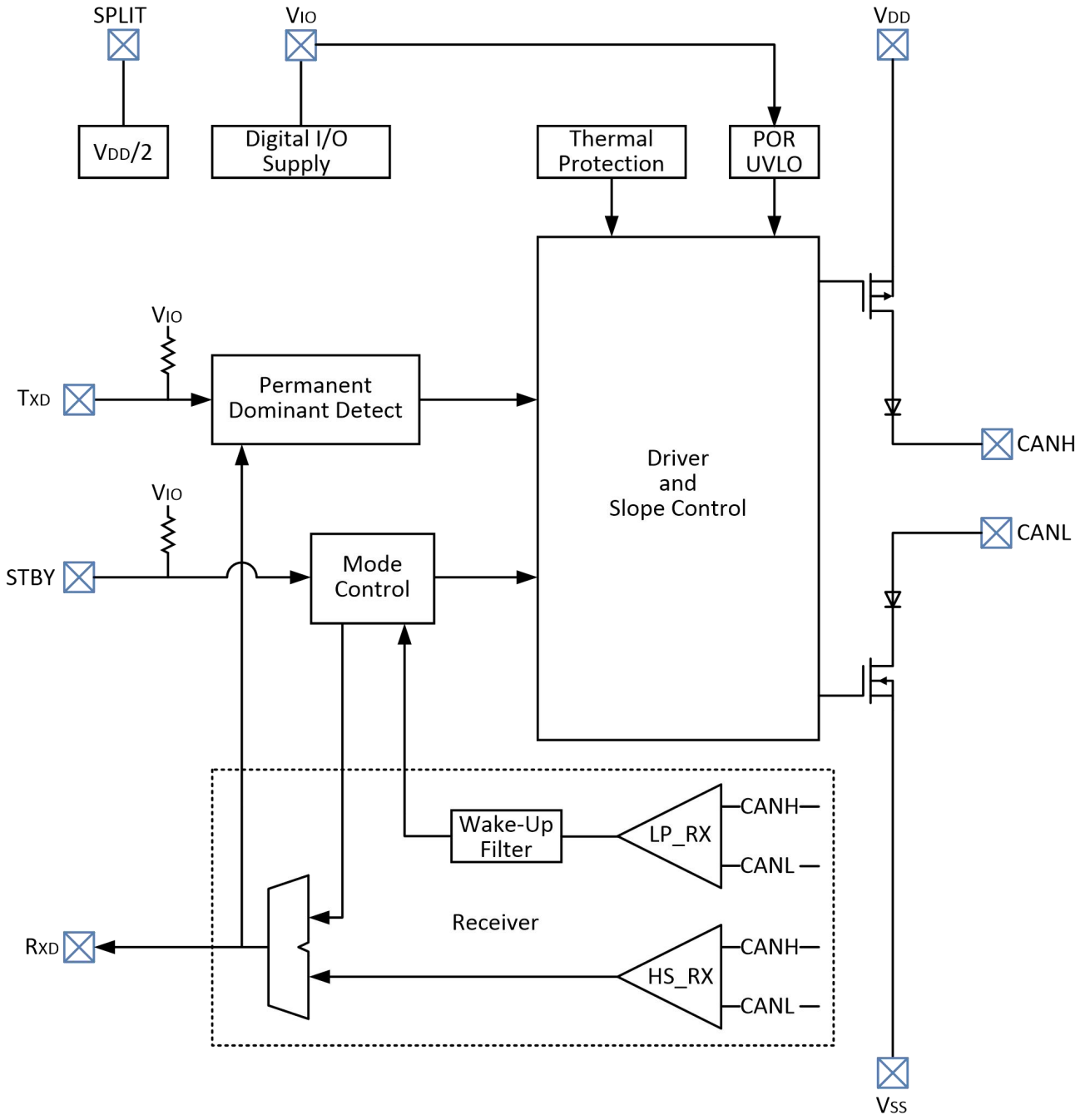
Figure 1 Pin Diagram

Pin Description

Pin	Name	Description
1	TXD	Transmit digital data input. LOW for dominant and HIGH for recessive bus states.
2	GND	Ground
3	V_{CC}	Supply voltage
4	RXD	Receive digital data output; reads out data from the bus lines, LOW for dominant and HIGH for recessive bus states.
5	SPLIT	Common-mode stabilization output; in COS1042T version only
5	V_{IO}	Supply voltage for I/O level adapter; in COS1042T/3 version only
6	CANL	LOW-level CAN bus I/O line
7	CANH	HIGH-level CAN bus I/O line
8	STB	Standby mode control input (Active high)

2. Ordering Information

Model	Order Number	Package	Package Option	Marking Information
COS1042	COS1042T	SOP-8	Tape and Reel, 4000	COS1042T
	COS1042T/3	SOP-8	Tape and Reel, 4000	COS1042T/3



Note 1: COS1042T has the SPLIT pin.
2: COS1042T/3 has the V_{IO} pin.

Figure 2. Block Diagram

3. Product Specification

3.1 Absolute Maximum Ratings (1)

Parameter	Min	Max	Unit
DC supply voltage V_{CC}	-0.3	7	V
DC supply voltage V_{IO}	-0.3	7	V
DC voltage at TXD, RXD, STB	-0.3	V_{IO} + 0.3	V
DC voltage at CANH, CANL and SPLIT	-44	+44	V
RXD output current	-8	+8	mA
Operating junction temperature	-40	+125	°C
Storage temperature	-55	+150	°C

(1) Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

3.2 Thermal Data

Parameter	Rating	Unit
Package Thermal Resistance	150 (SOP8) 90 (DIP8) 57 (DFN8,3x3)	°C/W

3.3 Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Unit
V_{CC} Supply voltage	4.5	5.0	5.5	V
V_{IO} Supply voltage on Pin V_{IO}	2.8	3.3	5.5	V
Operating ambient temperature	-40		+85	°C
Operating junction temperature	-40		+125	°C

3.4 DC Characteristics

(Typical values are tested at T_A=25 ºC, V_{CC}=4.5V to 5.5V, V_{IO}=2.8V to 5.5V, R_L=60Ω, unless otherwise specified.)

Parameter	Sym.	Conditions	Min.	Typ.	Max.	Unit
Vcc Supply						
Voltage range	V_{CC}		4.5	5.0	5.5	V
Undervoltage detection voltage	V_{UVD}		3.5	4.0	4.5	V
Hysteresis of UVD comparator	V_{UVDH}		0.3	0.5	0.8	V
Supply current	I_{CC}	Recessive; $V_{TXD}=V_{IO}$	-	4	10	mA
		Dominant; V_{TXD}=0V	-	22	40	mA
Standby current	I_{CCS}	COS1042T	-	12	17	μA
		COS1042T/3	-	-	1	μA
V_{IO} Supply						
Digital Supply voltage range	V_{IO}		2.8	-	5.5	V
Undervoltage detection voltage	V_{UVIO}		1.3	2.0	2.7	V
Supply current	I_{VIO}	Normal mode; V_{TXD}=0 or V_{IO}	-	20	200	μA
		Standby mode;	-	12	17	μA
BUS Line (CANH; CANL) Transmitter						
Standby mode output voltage	$V_{O(S)}$	Standby mode, no load	-0.1	0	+0.1	V
Recessive output voltage	$V_{O(R)}$	Normal mode, $V_{TXD}=V_{IO}$, no load	2	0.5V_{CC}	3	mV
Recessive Differential output voltage	$V_{O(DIFF)}$	$V_{TXD}=V_{IO}$	-50	0	50	mV
		$V_{TXD}=V_{IO}$, no load	-500	0	50	mV
Recessive Short circuit output current	$I_{O(SC)}$	Normal mode, $V_{CANH}=V_{CANH=}$-27V to +32V	-5		+5	mA
Dominant output voltage	$V_{O(D)}$	Pin CANH, V_{TXD}=0V	2.75	3.5	4.5	V
		Pin CANL, V_{TXD}=0V	0.5	1.5	2.25	V
Dominant Differential output voltage	$V_{O(DIFF)}$	Dominant, Normal mode, V_{TXD}=0V	1.5	2.0	3.0	V

Dominant Output voltage symmetry	$V_{O(D)(M)}$	V_{DD}-V_{CANH}-V_{CANL}	-400	0	400	mV
Dominant Short circuit output current	$I_{O(SC)}$	CANH; V_{TXD}=0, V_{CANH}=0V	-120	-70	-40	mA
		CANL; V_{TXD}=0, V_{CANL}=18V	40	85	120	mA
BUS Line (CANH; CANL) Receiver						
Recessive Differential input voltage	$V_{DIFF(RI)}$	Normal mode; −12V ≤ $V_{CANH,CANL}$ ≤ +12V;	-1.0	-	+0.5	V
		Standby mode; −12V ≤ $V_{CANH,CANL}$ ≤ +12V;	-1.0	-	+0.4	V
Dominant Differential input voltage	$V_{DIFF(DI)}$	Normal mode; −12V ≤ $V_{CANH,CANL}$ ≤ +12V;	0.9	-	V_{DD}	V
		Standby mode; −12V ≤ $V_{CANH,CANL}$ ≤ +12V;	1.0	-	V_{DD}	V
Differential Receiver Threshold	$V_{TH(DIFF)}$	Normal mode; −12V ≤ $V_{CANH,CANL}$ ≤ +12V;	0.5	0.7	0.9	V
		Standby mode; −12V ≤ $V_{CANH,CANL}$ ≤ +12V;	0.4	-	1.15	V
Differential Input Hysteresis	$V_{HYS(DIFF)}$	Normal mode	50	-	200	mV
Common mode input resistance	R_{IN}		10	15	25	kΩ
Common mode resistance matching	$R_{IN(M)}$		-1	-	+1	%
Differential input resistance	$R_{IN(DIFF)}$		20	30	50	kΩ
Common mode input capacitance	$C_{IN(CM)}$		-	-	20	pF
Differential input capacitance	$C_{IN(DIFF)}$		-	-	10	pF
Input leakage current	I_{LI}	V_{CC} = V_{TXD} = V_{STB} = 0V; V_{CANH} = V_{CANL} = 5V	-5		+5	μA
SPLIT; Common Mode Stabilization Output Pin (only for COS1042T)						
Output voltage	V_O	Normal mode; I_{SPLIT} = -500μA to +500μA	0.3V_{CC}	0.5V_{CC}	0.7V_{CC}	V
		Normal mode; R_L = 1MΩ	0.45V_{CC}	0.5V_{CC}	0.55V_{CC}	V
Leakage current	I_L	Standby mode; V_{SPLIT} = -24V to +24V	-5		+5	μA
TXD, STB Digital Input Pin						
HIGH-level input voltage	V_{IH}		0.7V_{IO}	-	V_{IO}+0.3	V
LOW-level input voltage	V_{IL}		-0.3	-	0.3V_{IO}	V
HIGH-level input current	I_{IH}		-1		+1	μA

TXD：LOW-level input current	$I_{IL(TXD)}$		-270	-150	-30	μA
STB：LOW-level input current	$I_{IL(STB)}$		-20	-	-1	μA
RXD Receive Data Output Pin						
HIGH-level output voltage	V_{OH}	I_{OH}=-4mA	V_{IO}-0.4	-	-	V
LOW-level output voltage	V_{OL}	I_{OL}=4mA	-	-	0.4	V
Thermal Shutdown						
Shutdown junction temperature	$T_{J(SD)}$		160	170	180	°C
Shutdown temperature Hysteresis	$T_{J(HYST)}$		20	30	40	°C

3.5 Dynamic Characteristics

(Typical values are tested at T_A=25 ºC, V_{CC}=4.5V to 5.5V, V_{IO}=1.8V to 5.5V, R_L=60Ω, unless otherwise specified. See Figure 6,7,8)

Parameter	Sym.	Conditions	Min.	Typ.	Max.	Unit
Delay TXD Low to bus dominant	$t_{TXD-BUSON}$	Normal mode	-	65	-	ns
Delay TXD High to bus recessive	$t_{TXD-BUSOFF}$	Normal mode	-	60	-	ns
Delay bus dominant to RXD	$t_{BUSON-RXD}$	Normal mode	-	65	-	ns
Delay bus recessive to RXD	$t_{BUSOFF-RXD}$	Normal mode	-	65	-	ns
Propagation delay TXD Low to RXD Low	$t_{TXDL-RXDL}$	Normal mode	-	-	220	ns
Propagation delay TXD High to RXD High	$t_{TXDH-RXDH}$	Normal mode	-	-	220	ns
Bus wake-up filter time	$t_{FLTR(WAKE)}$	Standby mode	0.5	1	4	μs
Delay standby to normal mode	t_{WAKE}	Negative edge on STB	2	3	10	μs
TXD dominant time-out time	$T_{to(dom)TXD}$	V_{TXD}=0V, Normal mode	0.3	2	5	ms
Bus dominant time-out time	$T_{to(dom)BUS}$	Standby mode	0.3	2	5	ms

4. Functional Description

4.1 Operating Mode

The COS1042 supports two operating modes, Normal and Standby, which are selected via pin STB. See Table 1 for a description of the operating modes under normal supply conditions.

Table 1. Operating Modes

Mode	STB	DRIVER	RECEIVER	RXD	
				LOW	HIGH
Normal	LOW	Enable (ON)	Enable (ON)	Bus dominant	Bus recessive
Standby	HIGH	Disable (OFF)	Only low power Bus monitor is active	Wake-up request detected	No wake-up request detected

4.1.1 Normal Mode

A LOW level on pin STB selects Normal mode. In this mode, the transceiver can transmit and receive data via the bus lines CANH and CANL (see Figure 2 for the block diagram). The differential receiver converts the analog data on the bus lines into digital data which is output to pin RXD. The slopes of the output signals on the bus lines are controlled internally and are optimized in a way that guarantees the lowest possible EME.

4.1.2 Standby Mode

A HIGH level on pin STB selects Standby mode. In Standby mode, the transceiver is not able to transmit or correctly receive data via the bus lines. The transmitter and Normal-mode receiver blocks are switched off to reduce supply current, and only a low-power differential receiver monitors the bus lines for activity. The wake-up filter on the output of the low-power receiver does not latch bus dominant states, but ensures that only bus dominant and bus recessive states that persist longer than $t_{fltr(wake)bus}$ are reflected on pin RXD. In Standby mode, the bus lines are biased to ground to minimize the system supply current. The low-power receiver is supplied by V_{IO}, and is capable of detecting CAN bus activity even if V_{IO} is the only supply voltage available. When pin RXD goes LOW to signal a wake-up request, a transition to Normal mode will not be triggered until STB is forced LOW.

4.2 Fail-Safe Features

4.2.1 TXD Dominant Time-out Function

A ‘TXD dominant time-out’ timer is started when pin TXD is set LOW. If the LOW state on pin TXD persists for longer than $t_{to(dom)TXD}$, the transmitter is disabled, releasing the bus lines to recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when pin TXD is set to HIGH. The TXD dominant time-out time also defines the minimum possible bit rate of 40 kbit/s.

4.2.2 Bus Dominant Time-out Function

In Standby mode a 'bus dominant time-out' timer is started when the CAN bus changes from recessive to dominant state. If the dominant state on the bus persists for longer than $t_{to(dom)bus}$, the RXD pin is reset to HIGH. This function prevents a clamped dominant bus (due to a bus short-circuit or a failure in one of the other nodes on the network) from generating a permanent wake-up request. The bus dominant time-out timer is reset when the CAN bus changes from dominant to recessive state.

4.2.3 Internal Biasing of TXD and STB Input Pins

Pins TXD and STB have internal pull-ups to V_{IO} to ensure a safe, defined state in case one or both of these pins are left floating. Pull-up currents flow in these pins in all states; both pins should be held HIGH in Standby mode to minimize standby current.

4.2.4 Undervoltage Detection on Pins Vcc and V_{IO}

Should V_{CC} drop below the V_{CC} undervoltage detection level, $V_{UVD(VCC)}$, the transceiver will switch to Standby mode. The logic state of pin STB will be ignored until VCC has recovered. Should V_{IO} drop below the V_{IO} undervoltage detection level, $V_{UVD(VIO)}$, the transceiver will switch off and disengage from the bus (zero load) until V_{IO} has recovered.

4.2.5 Over-temperature Protection

The output drivers are protected against over-temperature conditions. If the virtual junction temperature exceeds the shutdown junction temperature, Tj(sd), the output drivers will be disabled until the virtual junction temperature falls below Tj(sd) and TXD becomes recessive again. Including the TXD condition ensures that output driver oscillation due to temperature drift is avoided.

4.2.6 Unpowered Device

The COS1042 is designed to be “ideal passive” or “no load” to the CAN bus if it is unpowered. The bus terminals (CANH, CANL) have extremely low leakage currents when the device is unpowered to avoid loading down the bus. This is critical if some nodes of the network are unpowered while the rest of the of network remains in operation. The logic terminals also have extremely low leakage currents when the device is unpowered to avoid loading down other circuits that may remain powered.

4.2.7 Floating Terminals

The COS1042 has internal pull ups on critical terminals to place the device into known states if the terminals float. The TXD terminal is pulled up to V_{CC} or V_{IO} to force a recessive input level if the terminal floats. The STB terminal is also pulled up to force the device into low power Standby mode if the terminal floats.

4.2.8 CAN Bus Short Circuit Current Limiting

The COS1042 has The device has two protection features that limit the short circuit current when a CAN bus line is short-circuit fault condition: driver current limiting (both dominant and recessive states) and TXD dominant state time out to prevent permanent higher short circuit current of the dominant state during a system fault.

4.3 SPLIT Output Pin and V_{IO} Supply Pin

Two versions of the COS1042 are available, only differing in the function of a single pin. Pin 5 is either a SPLIT output pin or a V_{IO} supply pin. Using the SPLIT pin on the COS1042T in conjunction with a split termination network (see Figure 3 and Figure 4) can help to stabilize the recessive voltage level on the bus. This will reduce EME in networks with DC leakage to ground (e.g. from deactivated nodes with poor bus leakage performance). In Normal mode, pin SPLIT delivers a DC output voltage of $0.5V_{CC}$. In Standby mode or when V_{CC} is off, pin SPLIT is floating. When not used, the SPLIT pin should be left open.

Pin V_{IO} on the COS1042T/3 should be connected to the micro-controller supply voltage (see Figure 5). This will adjust the signal levels of pins TXD, RXD and STB to the I/O levels of the micro-controller. Pin V_{IO} also provides the internal supply voltage for the low-power differential receiver of the transceiver. For applications running in low-power mode, this allows the bus lines to be monitored for activity even if there is no supply voltage on pin V_{CC}. For versions of the COS1042 without a V_{IO} pin, the V_{IO} input is internally connected to VCC. This sets the signal levels of pins TXD, RXD and STB to levels compatible with 5 V micro-controllers.

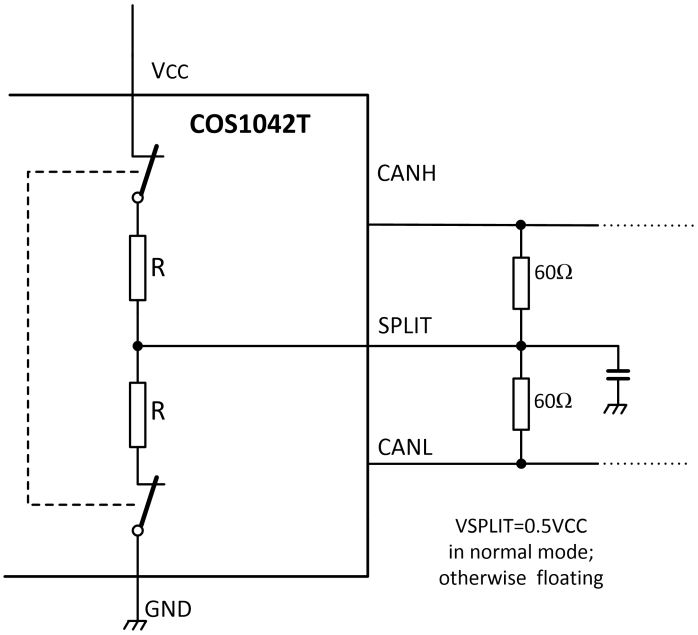


Figure 3. Stabilization Circuitry and Application for Version with SPLIT Pin

5. Typical Application Diagrams

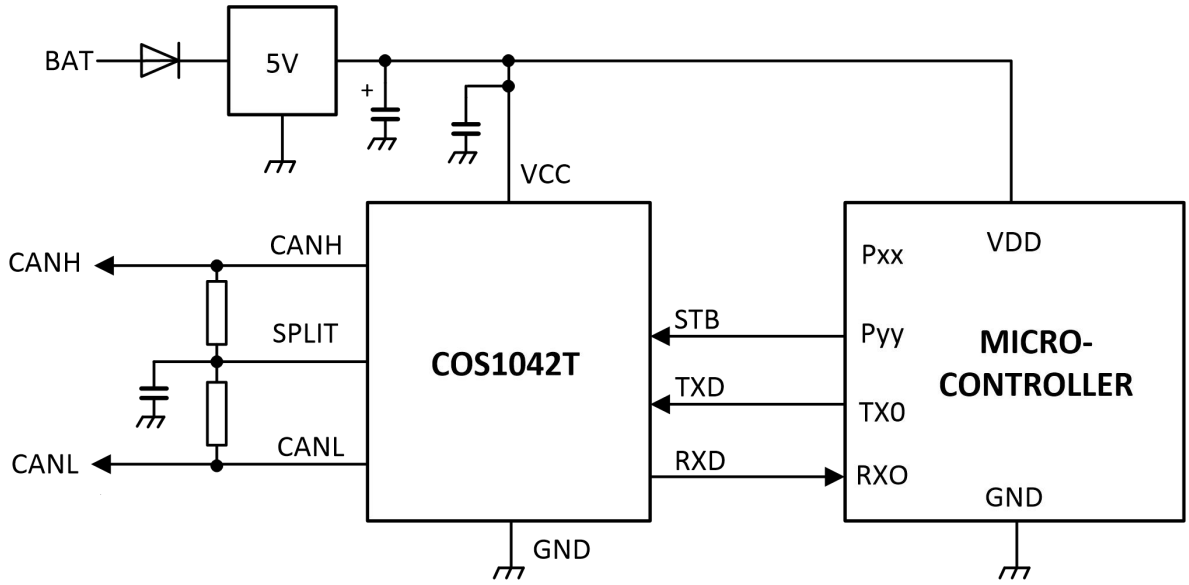


Figure 4. Typical Application with COS1042T and a 5V Micro-controller

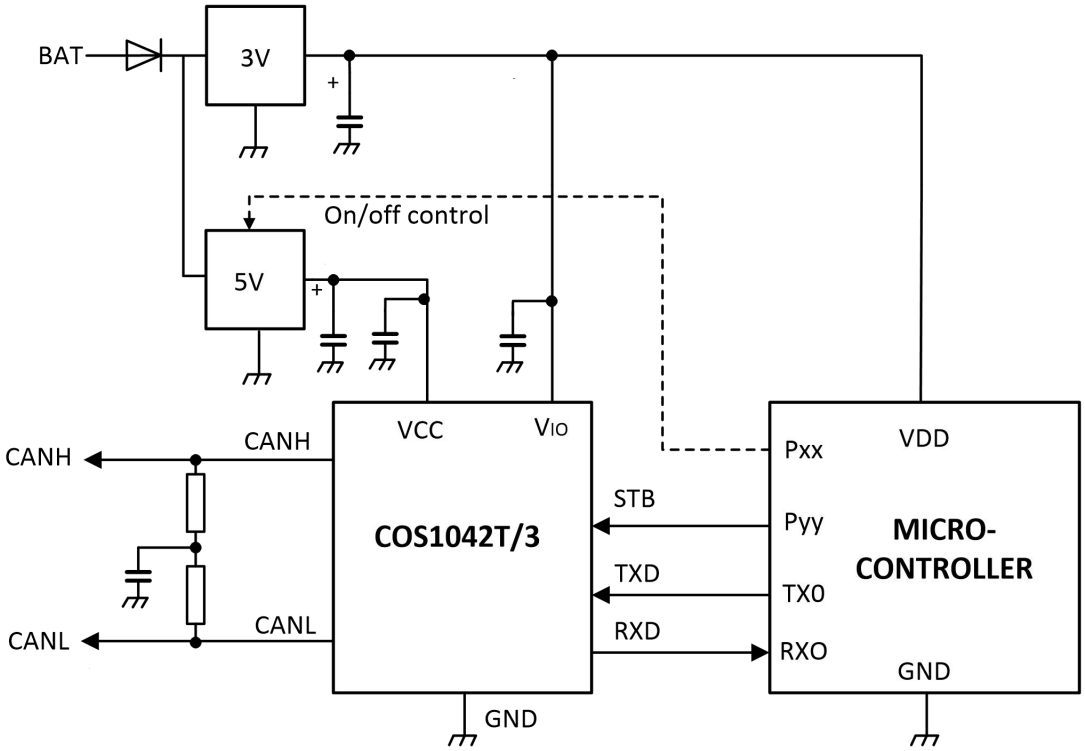


Figure 5. Typical Application with COS1042T/3 and a 3V Micro-controller

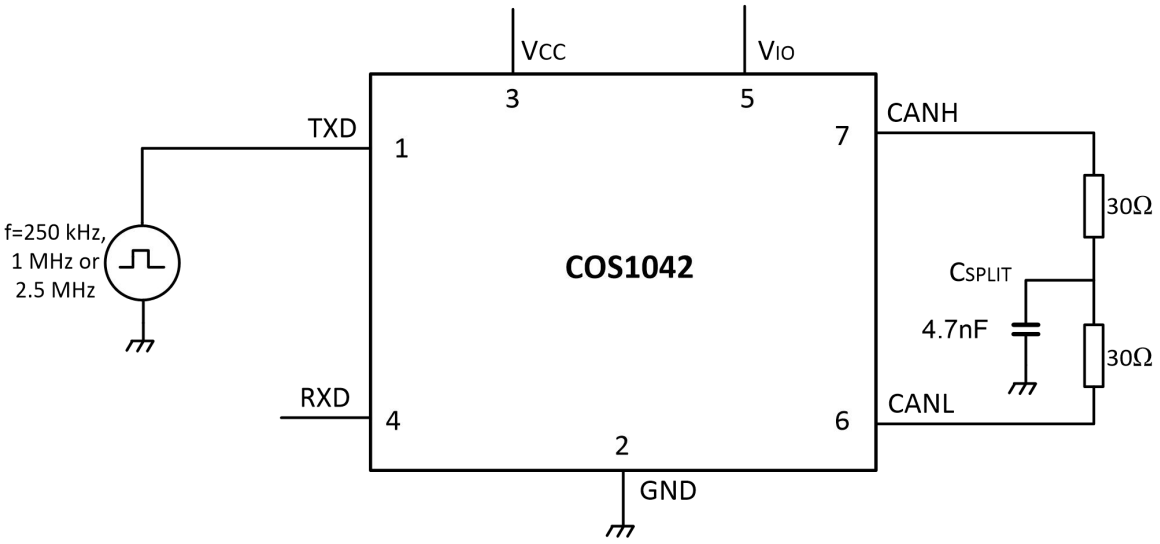


Figure 6. Test Circuit for Measuring Transceiver Driver Symmetry

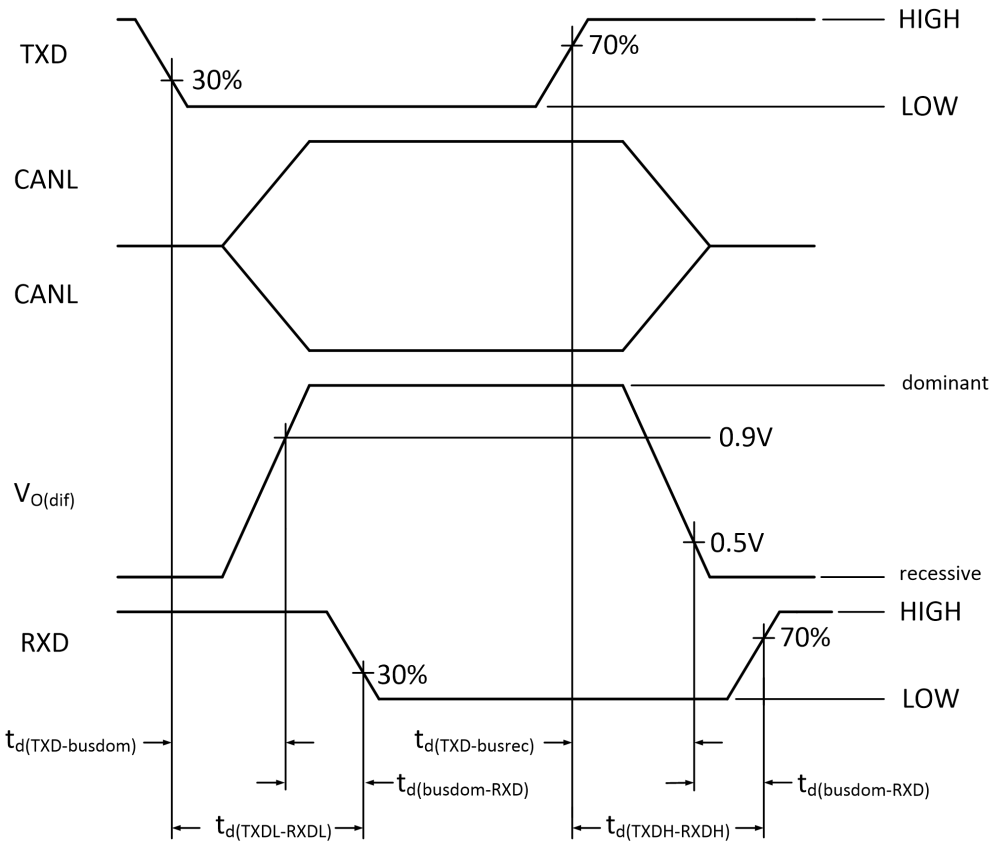


Figure 7. CAN Transceiver Timing Diagram

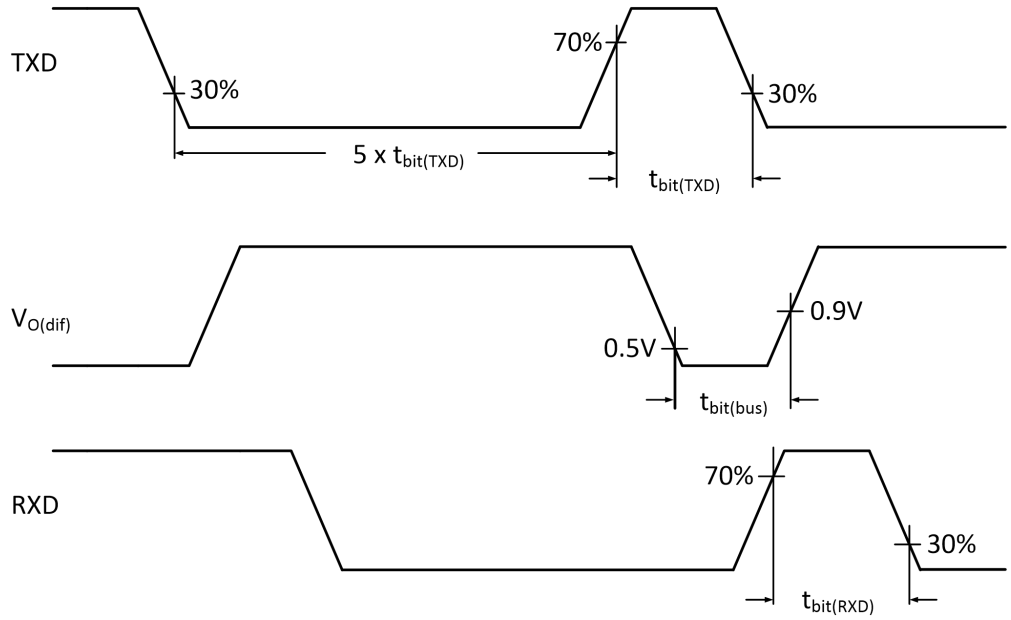
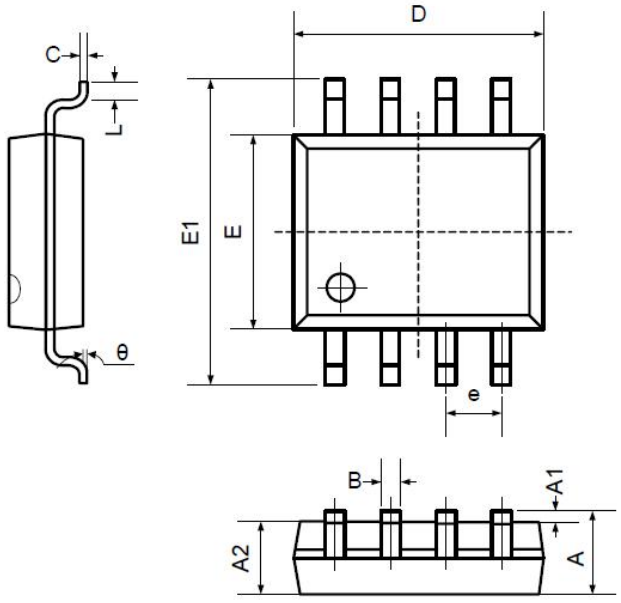


Figure 8. CAN FD Timing Definition According to ISO11898-2

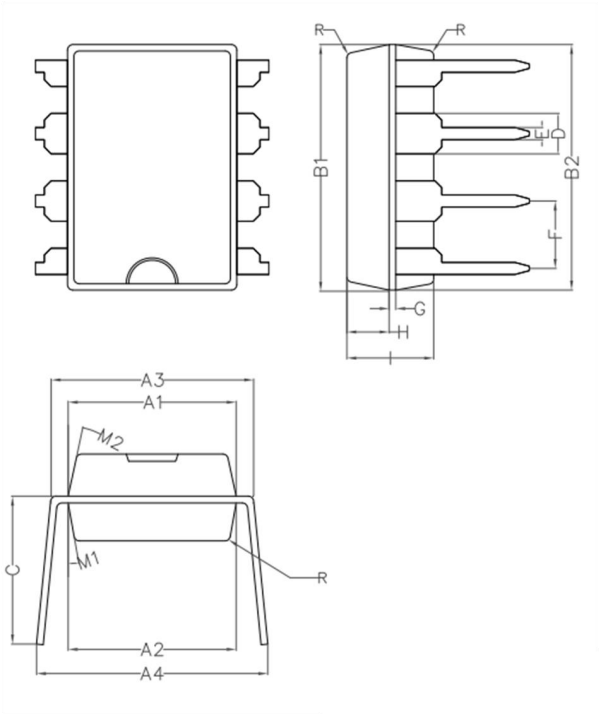
6. Package Information

6.1 SOP8 (Package Outline Dimensions)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

6.2 DIP8 (Package Outline Dimensions)



Symbol	Min	Non	Max
A1	6.28	6.33	6.38
A2	6.33	6.38	6.43
A3	7.52	7.62	7.72
A4	7.80	8.40	9.00
B1	9.15	9.20	9.25
B2	9.20	9.25	9.30
C		5.57	
D		1.52	
E	0.43	0.45	0.47
F		2.54	
G		0.25	
H	1.54	1.59	1.64
I	3.22	3.27	3.32
R		0.20	
M1	9°	10°	11°
M2	11°	12°	13°